WHAT IS CLAIMED IS:

1. A semiconductor integrated circuitry comprising:

a first MISFET including gate electrodes formed on a main surface of a semiconductor substrate via a gate insulating film;

a first semiconductor area in contact with a channel area formed under said gate electrodes on the main surface of said semiconductor substrate;

a second MISFET including gate electrodes formed on the main surface of the semiconductor substrate via said gate insulating film;

a low density semiconductor area in contact with a channel area formed under said gate electrodes on the main surface of said semiconductor substrate;

and a high density semiconductor area formed outside said low density semiconductor area,

wherein a cap insulating film is formed on top of said gate electrodes of said first and second MISFETS, first side walls formed with first insulating film are formed on side surfaces of said gate electrodes of said second MISFET, second side walls formed with second insulating film comprised of a different member from that of said first insulating film are formed outside said first side walls, a conductor portion connecting said first semiconductor area to a member formed in an upper layer of said first MISFET is formed in a self-aligning manner with respect to third side walls formed with said first insulating film and on side surfaces of the gate electrodes of said first MISFET, and

wherein said high density semiconductor area is formed in a self-aligning manner with respect to said second side walls formed with said second insulating film.

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2. A semiconductor integrated circuitry as defined in claim 1, wherein said first insulating film forms first and third side wall spacers comprised of a silicon nitride film formed on side surfaces of said first and second MISFET gate electrodes and said second insulating film forms second side wall spacers comprised of a silicon oxide film formed on side surfaces of said second MISFET gate electrodes with said first side wall spacers therebetween.

3. A semiconductor integrated circuitry as defined in claim 1, wherein said first insulating film is a silicon nitride film formed on said semiconductor substrate including side surfaces of said gate electrodes and said second insulating film is a silicon oxide film formed on side surfaces of said gate electrodes with said silicon nitride film therebetween.

4. A semiconductor integrated circuitry as defined in claim 1, wherein said second MISFET includes an N channel MISFET and a P channel MISFET and has a CMISFET structure.

5. A semiconductor integrated circuitry as defined in claim 1 wherein said first MISFET is a selecting MISFET of a DRAM disposed in a memory array area of DRAM cells and said member formed in the upper layer of said first MISFET is a DRAM storage capacitor or a bit line.

6. A semiconductor integrated circuitry as defined in claim 5, wherein an impurity doped in the semiconductor area of said selecting MISFET is phosphorus

and the low density or high density semiconductor area of said N channel MISFET of said second MISFET is doped at least with arsenic.

7. A semiconductor Integrated circuitry as defined in claim 6, wherein said N channel MISFET includes a first N channel MISFET and a second N channel MISFET, and said first N channel MISFET includes an arsenic doped low density semiconductor area and an arsenic doped high density semiconductor area, and said second N channel MISFET includes a phosphorus doped low density semiconductor area and an arsenic doped high density semiconductor area.

8. A semiconductor integrated circuitry as defined in claim 7, wherein said first N channel MISFET includes a boron doped semiconductor area in contact with said high density semiconductor area under said low density semiconductor area and said second N channel MISFET does not include said boron doped semiconductor area.

9. A semiconductor integrated circuitry as defined in claim 6, wherein a silicide layer is not formed on the surface of said semiconductor area of said selecting MISFET and a silicide layer is formed on the surface of said high density semiconductor area of said second MISFET is formed a silicide layer.

10. A semiconductor integrated circuitry as defined in claim 5, wherein said gate insulating film of said selecting MISFET is thicker than that of said second MISFET.

11. A semiconductor integrated circuitry as defined in claim 1, wherein said first MISFET, in which the gate insulating film thereof is a tunnel insulating film, is a floating gate type MISFET disposed in a memory array area of nonvolatile memory cells including control gate electrodes formed on the gate insulating film via floating gate electrodes and separated from said floating gate electrodes via an insulating film.

12. A semiconductor integrated circuitry as defined in claim 11, wherein said gate insulating film of said second MISFET is thicker than that of said first MISFET.

13. A semiconductor integrated circuitry as defined in claim 5, wherein said first MISFET includes said selecting MISFET and said floating gate type MISFET.

14. A semiconductor integrated circuitry as defined in claim 13, wherein said DRAM bit line and a wiring formed in the upper layer of said floating gate type MISFET are formed In the same process.

15. A semiconductor integrated circuitry as defined in claim 13, wherein gate insulating films of said selecting MISFET, said floating gate type MISFET, a peripheral circuit or logic circuit MISFET that drives said DRAM, and said peripheral circuit MISFET that drives said floating gate type MISFET are different in thickness from each other and said gate insulating film of said peripheral circuit MISFET that drives said floating gate type MISFET is thicker than that of said floating gate type MISFET and said gate insulating film of said floating gate type MISFET is thicker

than that of said selecting MISFET, and said gate insulating film of said selecting MISFET is thicker than that of said peripheral circuit or logic circuit MISFET that drives said DRAM.

16. A semiconductor integrated circuitry as defined in claim 15, wherein, in an area where said second MISFET is formed, a silicon nitride film is also formed covering said second MISFET and said semiconductor substrate.